In The Claims:

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1. (Currently Amended) An apparatus for executing block data transfer instruction inside a processor after receiving decode information containing N bits, the apparatus comprising:

an adder for receiving the N-bit decode information and adding the N bits together to produce an initial count value;

a counter for receiving the initial count value, decreasing the value by one after outputting a count control signal;

a register identification number generator that generates a plurality of register identification numbers equal in number to the initial count value according to the count control signal, wherein the register identification number corresponds to the bit positions in the N-bit decode information having a bit value '1';

a memory unit for holding data; and

a register list that includes a plurality of registers, wherein the register list is able to receive the register identification numbers so that stored data can be freely exchanged between the memory unit and the registers [~~having the corresponding~~]that correspond to the register identification numbers.

2. (Original) The apparatus of claim 1, wherein the apparatus further includes an address calculator for generating an address signal according to the decode information and then outputting the address signal to the memory unit so that data can be freely exchanged between

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the registers that correspond to the register identification numbers and the addressed memory in the memory unit according to the address signal.

3. (Original) The apparatus of claim 1, wherein the register identification number generator further includes N logic units for generating register identification numbers equal in number to the initial count value such that when the counter decrements by one down to zero, the N logic unit is able to generate corresponding register identification number according to the bit position in the N-bit decode information that has a value '1'.

4. (Currently Amended) A method of executing block data transfer instruction inside a processor after receiving an N-bit decode information, comprising the steps of:

adding the N bits together to form an initial count value;

generating a plurality of register identification number identical in number to the initial count value, wherein the register identification number corresponds to the bit position of the N-bit decode information that has a bit value '1'; and

[~~linking up~~]mapping the plurality of registers that correspond to the register identification numbers [~~and~~]to the memory unit according to the register identification numbers so that stored data can be exchanged between the memory unit and the registers.

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5. (Original) The method of claim 4, wherein the step for generating the register identification numbers includes the sub-steps of:

performing a count down operation decreasing the initial value count by one until the value zero is reached; and

generating a register identification number whenever a bit value of '1' is found in the N-bit decode information after each count down operation.

6. (Original) The method of claim 4, wherein the method further includes generating an address signal according to the decode information so that stored data in the register corresponding to the register identification number and data within the memory unit having an address corresponding to the address signal can exchange with each other.